CLAIMS

WHAT IS CLAIMED:

1. A device, comprising:

a transistor comprising a charge trapping area, wherein a threshold voltage of said transistor is modified upon trapping of charges in said charge trapping unit;

a memory element; and

a fuse associated with said memory element, said fuse to enter in an alternative state in response to modifying said threshold voltage of said transistor, thereby at least one of programming and de-programming said memory element.

2. The device of claim 1, wherein said device is a memory device.

3. The device of claim 2, wherein said memory device is at least one of a static random access memory (SRAM), a pseudo-static static random access memory (PSRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.

4. The device of claim 1, wherein said transistor is an N-channel device.

5. The device of claim 1, wherein said transistor is coupled to a plurality of conductive lines.

6. The device of claim 5, wherein at least one of said plurality of conductive lines is coupled to ground.

7. The device of claim 1, wherein at least one of said plurality of conductive lines is coupled to a programmable voltage.

8. The device of claim 1, wherein said threshold voltage is modified by an increase of about 100 millivolts.

9. The device of claim 1, wherein said threshold voltage is modified by an increase of about 200 millivolts.

10. The device of claim 1, wherein said transistor comprises an LDD region proximate a source region and a masked-off region proximate a drain region to prevent an LDD region proximate said drain region.

11. A circuit for performing a redundancy programming, comprising:

an access transistor comprising a charge trapping area, wherein a threshold voltage of said access transistor is modified upon trapping of charges in said charge trapping unit;

a memory element; and

a fuse associated with said memory element, said fuse to become blown in response to modifying said threshold voltage of said access transistor, thereby de-programming said memory element.

12. The circuit of claim 11, wherein said access transistor is an N-channel device.

13. The circuit of claim 11, further comprising a plurality of conductive lines.

14. The circuit of claim 13, wherein at least one of said plurality of conductive lines is coupled to ground.

15. The circuit of claim 11, wherein at least one of said plurality of conductive lines is coupled to a programmable voltage.

16. The circuit of claim 11, wherein said access transistor comprises an LDD region proximate a source region and a masked-off region proximate a drain region to prevent an LDD region proximate said drain region.

17. A system board, comprising:

a controller for performing a memory operation; and

a memory device operatively coupled to said controller, said memory device to provide memory access to said controller, said memory device comprising:

an access transistor comprising a charge trapping area, wherein a threshold voltage of said access transistor is modified upon trapping of charges in said charge trapping unit;

a memory element; and

a fuse associated with said memory element, said fuse to become blown in response to modifying said threshold voltage of said

access transistor, thereby de-programming said memory element.

18. The system board of claim 17, wherein said memory device is at least one of a static random access memory (SRAM), a pseudo-static static random access memory (PSRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.

19. The system board of claim 18, wherein said access transistor is an N-channel device.

20. The system board of claim 18, wherein said access transistor is coupled to a plurality of conductive lines.

21. The system board of claim 20, wherein at least one of said plurality of conductive lines is coupled to ground.

22. The system board of claim 21, wherein at least one of said plurality of conductive lines is coupled to a programmable voltage.

23. The system board of claim 17, wherein said access transistor comprises an LDD region proximate a source region and a masked-off region proximate a drain region to prevent an LDD region proximate said drain region.

24. A system for performing a redundant memory programming, comprising:

a device testing unit for performing a memory test;

a memory device operatively coupled to said device testing unit, said memory device comprising:

an access transistor comprising a charge trapping area, wherein a threshold voltage of said access transistor is modified upon trapping of charges in said charge trapping unit;

a memory element; and

a fuse associated with said memory element, said fuse to enter in an alternative state in response to modifying said threshold voltage of said access transistor by said device testing unit, thereby at least one of programming and de-programming said memory element.

25. The system of claim 24, wherein said device testing unit comprising:

a redundant programming unit capable of modifying said threshold voltage for performing said redundant memory programming; and

a sense unit capable of sensing the threshold voltage of said access transistor.

26. The system of claim 24, wherein said sense unit comprises at least one sense amplifier.

27. The system of claim 24, wherein said memory device is at least one of a static random access memory (SRAM), a pseudo-static static random access memory (PSRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.

28. The system of claim 24, wherein said access transistor is an N-channel device.

29. The system of claim 24, wherein said access transistor is coupled to a plurality of conductive lines.

30. The system of claim 29, wherein at least one of said plurality of conductive lines is coupled to ground.

31. The system of claim 24, wherein at least one of said plurality of conductive lines is coupled to a programmable voltage.

32. The system of claim 24, wherein said threshold voltage is modified by an increase of about 100 millivolts.

33. The system of claim 24, wherein said threshold voltage is modified by an increase of about 200 millivolts.

34. The system of claim 24, wherein said memory device comprises:

a first fuse set comprising a plurality of fuses;

a first memory cell associated with said first fuse set, wherein a charge trapping may be performed upon said memory cell based upon de-activation of at least one fuse in said first fuse set;

a second fuse set comprising a plurality of fuses; and

a second memory cell associated with said second fuse set, wherein a charge trapping may be performed upon said memory cell based upon de-activation of at least one fuse in said second fuse set.

35. The system of claim 34, wherein said first fuse set comprises four fuses that may be controlled for activating one of a plurality of memory elements associated with said first memory cell.

36. The system of claim 35, wherein said second fuse set comprises four fuses that may be controlled for activating one of a plurality of memory elements associated with said second memory cell.

37. The system of claim 24, wherein said access transistor comprises an LDD region proximate a source region and a masked-off region proximate a drain region to prevent an LDD region proximate said drain region.

38. A method, comprising:

programming a memory element in a memory device by controlling a threshold voltage associated with said memory device, controlling said threshold voltage comprising controlling the threshold voltage of an access transistor by

trapping charges in a charge trapping area of said access transistor, wherein a threshold voltage of said access transistor is modified upon trapping of charges in said charge trapping unit, wherein programming said memory element further comprises activating a fuse coupled to said memory element in response to said changing said threshold voltage, for activating said memory element.

39. The method of claim 38, further comprising:

grounding a gate terminal of said access transistor;

grounding a substrate of said threshold voltage; and

providing a high voltage upon a drain terminal of said access transistor to perform trapping of charges into an overlap region of a region associated with said drain terminal.

40. The method of claim 38, further comprising:

sensing a first conduction level associated with a first memory element of said memory device;

sensing a second conduction level associated with a second memory element of said memory device; and

comparing said first and second conduction levels to determine whether at least one of said first memory element and said second memory element is active.

41. The method of claim 40, further comprising activating said first memory element by modifying a level of a threshold associated with said first memory element.

42. The method of claim 40, further comprising de-activating said second memory element by modifying a level of a threshold associated with said second memory element.

43. The method of claim 38, further comprising modifying said threshold voltage by an increase of about 100 millivolts.

44. The method of claim 38, further comprising modifying said threshold voltage by an increase of about 200 millivolts.

45. An apparatus, comprising:

means for programming a memory element in a memory device by controlling a threshold voltage associated with said memory device, means for controlling said threshold voltage comprising means for controlling the threshold voltage of an access transistor by trapping charges in a charge trapping area of said access transistor, wherein a threshold voltage of said access transistor is modified upon trapping of charges in said charge trapping unit, wherein means for programming said memory element further comprises means for activating a fuse coupled to said memory element in response to said changing said threshold voltage, for activating said memory element.